AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph 3 of Page 1, beginning at Line 19 and continuing onto Page 2 with the following amended paragraph:

ESD efficiency is typically measured by dividing the ESD "threshold" voltage by the area of the ESD protection device as described in the report by Chen et al., "Design and Layout of High ESD Performance NPN Structure for Subrmicron BiCMOS/Bipoiar Circuits.", ~~IIIE Journal, 1996 0-7803-2753-5/96~~34th Annual Proceedings of the IEEE International Symposium on Reliability Physics, pp. 227-232, 1996. ESD threshold can be correlated to the secondary breakdown characteristic of the bipolar transistor as depicted in Fig. 1. The initial collector base breakdown (Bvcbo) initiates the device turn on which is followed by breakdown of collector to emitter (BVceo) as conduction enters the avalanche region between BVceo and Vt2, It2. Vt2 and It2 define the beginning of the secondary breakdown region in which the npn can be damaged due to Joule heating of the collector base junction. The higher the It2, that is the current threshold prior to secondary breakdown, the higher the ESD threshold, the better the ESD characteristics of the device. It is found that an increase in It2 and hence ESD threshold, scales with emitter length. However, as emitter length is increased there is a corresponding increase in device area. This takes up valuable active circuit area, and results in increased device capacitance which is detrimental in high speed circuit operation. In an effort to control or reduce ESD device area while maintaining or improving ESD efficiency, prior art designs have used multiple emitter finger designs. The top view horizontal layout of one such design is depicted in Fig 4. It is seen in Fig. 4 that there are N+1 base conductors 20 for every N emitter fingers 28. In the case shown, N=4 and therefore there are 5 base connections 20 running in a horizontal interdigitated fashion between the emitter fingers 28.

Please replace the paragraph from the beginning of Page 6 and continuing onto Page 7 with the following amended paragraph:

Fig. 2 depicts a vertical cross section of a multiple element bipolar ESD protection device. The starting structure is a p doped substrate 10, typically created on a silicon wafer of 100 crystal orientation and with a doping level in the range of 10^{15} atoms per cubic centimeter (a/cm^3). A heavily doped n+ first semiconductor layer 12 called a buried layer or subcollector is formed upon the substrate typically using arsenic or antimony as impurity ~~dopents~~dopants and using either a chemical diffusion or an ion implant process. An ion implant process typically uses an implant energy in the range of 30 KeV with a dosage of 10^{15} atoms per square centimeter (a/cm^2) to produce a n+ ~~buried layer~~region doping level between 10^{18} and 10^{19} a/cm^3. Next, a light to moderately doped n type epitaxial second semiconductor layer 14 is deposited with a doping level typically in the range of 10^{15} to 10^{16} a/cm^3 with arsenic frequently being used as the ~~dopent~~dopant source element. A plurality of deep n+ regions 16 are implanted into the second semiconductor layer 14 beneath the collector contact regions 18 typically using either an arsenic, antimony or phosphorous ~~dopent~~dopant with an implant energy in the range of 30 KeV with a dosage of 10^{15} a/cm^2 to produce an n+ buried layer doping level between 10^{18} and 10^{19} a/cm^3. This provides a low resistance path to the surface conductor system 34 for the collector current. The structure processing is continued by implanting a third semiconductor layer 24 of p ~~dopent~~dopant, usually boron, with an implant energy in the range of 30 KeV with a dosage of 10^{14} a/cm^2 to produce a p layer with a typical impurity concentration in a range of between 10^{17} and 10^{18} a/cm^3 to form the transistor base regions. This is followed by implanting a plurality of p+ regions 22 using boron as a source with doping levels typically between 10^{18} and 10^{19} a/cm^3 within the third semiconductor layer base region 24 to form high conductivity regions for the base electrical contacts 20. Next, a plurality of third n doped semiconductor regions 26 is implanted, typically with phosphorous, with an implant energy in the range of 30 KeV and with a

dosage of between 10^{16} and 10^{17} a/cm^2 to produce a p layer with a typical impurity concentration in a range of between 10^{19} and 10^{20} a/cm^3 for the transistor emitter regions 26. The electrical contacts with the surface conductors for the collector 18, base 20, and emitter 28 are typically made by using a refractory metal silicide such as titanium silicide ($TiSi_2$) or tungsten silicide ~~(Wsi_2)~~(WSi_2) together with doped polysilicon (poly) or aluminum conductor elements.

Please replace the last paragraph beginning on line 11 of Page 10 with the following amended paragraph:

What is claimed is: